What is claimed is:

1. A deep trench self-alignment process for an active area of a partial vertical cell, comprising:

providing a semiconductor substrate having two deep trenches;

forming a deep trench capacitor in each deep trench, lower than the top surface of the semiconductor substrate;

forming an isolating layer covering each deep trench capacitor;

filling a mask layer in each deep trench;

forming a photoresist layer covering the semiconductor substrate between the deep trenches, wherein the mask layer surface is partially covered by the photoresist layer;

etching the semiconductor substrate using the photoresist layer and the mask layers as etching masks to below the isolating layer; and

removing the photoresist layer and the mask layers, wherein the pillared semiconductor substrate between the deep trenches act as an active area.

2. The deep trench self-alignment process for an active area of a partial vertical cell of claim 1, wherein a ring-shaped insulating layer is formed on a top sidewall of each deep trench.

3. The deep trench self-alignment process for an active area of a partial vertical cell of claim 2, wherein the ring-shape insulating layer is a collar oxide layer.

4. The deep trench self-alignment process for an active area of a partial vertical cell of claim 1, wherein the isolating layer is an oxide layer.

5. The deep trench self-alignment process for an active area of a partial vertical cell of claim 1, wherein the mask layer is an anti-reflection coating layer.

6. The deep trench self-alignment process for an active area of a partial vertical cell of claim 1, wherein the etching is carried out using a gas mixture containing HBr and oxygen.

7. The deep trench self-alignment process for an active area of a partial vertical cell of claim 1, wherein the etching is anisotropic.

8. The deep trench self-alignment process for an active area of a partial vertical cell of claim 8, wherein the anisotropic etching is plasma or reactive ion etching.

9. A deep trench self-alignment process for an active area of a partial vertical cell, comprising:

providing a semiconductor substrate, wherein a pad layer is formed covering the semiconductor substrate;

forming two deep trenches in the semiconductor substrate separated by a predetermined distance;

forming a deep trench capacitor in each deep trench, wherein the deep trench capacitors are below the top surface of the semiconductor substrate, and a ring-shaped insulating layer is formed on a top sidewall of each deep trench;

conformally forming an isolating layer covering the semiconductor substrate and the deep trenches;

removing the isolating layer from the sidewall of the deep trench to leave the isolating layer on the deep trench capacitor;

forming a mask layer covering the semiconductor substrate, wherein the deep trench is filled with the mask layer;

planarizing the mask layer until the semiconductor substrate is exposed to leave the mask layer in the deep trenches;

forming a photoresist layer covering the semiconductor substrate between the deep trenches, wherein the mask layer is partially covered by the photoresist layer;

etching the semiconductor substrate to a predetermined depth using the photoresist layer and the mask layer as etching masks; and

removing the photoresist layer and the mask layer, wherein a pillared semiconductor substrate between the deep trenches act as an active area.

10. The deep trench self-alignment process for an active area of a partial vertical cell of claim 9, wherein the pad layer is a pad oxide layer or a pad nitride layer.

11. The deep trench self-alignment process for an active area of a partial vertical cell of claim 9, wherein the predetermined distance between the deep trenches is about 1200 to 1400Å.

12. The deep trench self-alignment process for an active area of a partial vertical cell of claim 9, wherein the ring-shape insulating layer is a collar oxide layer.

13. The deep trench self-alignment process for an active area of a partial vertical cell of claim 9, wherein the isolating layer is an oxide layer.

14. The deep trench self-alignment process for an active area of a partial vertical cell of claim 9, wherein removal uses anisotropic etching.

15. The deep trench self-alignment process for an active area of a partial vertical cell of claim 9, wherein the mask layer is an anti-reflection coating layer.

16. The deep trench self-alignment process for an active area of a partial vertical cell of claim 9, wherein planarization uses chemical mechanical polishing or etching.

17. The deep trench self-alignment process for an active area of a partial vertical cell of claim 9, wherein the etching is carried out using a gas mixture containing HBr and oxygen.

18. The deep trench self-alignment process for an active area of a partial vertical cell of claim 9, wherein the etching is anisotropic.

19. The deep trench self-alignment process for an active area of a partial vertical cell of claim 18, wherein the anisotropic etching is plasma etching or reactive ion etching.

20. The deep trench self-alignment process for an active area of a partial vertical cell of claim 9, where the predetermined depth is about 2600 to 3000Å.